

CS 573
Final Exam
May 2, 2005

READ THESE INSTRUCTIONS

The following exam is open book and open notes. You may feel free to use whatever additional reference material you wish, but **no electronic aids** are allowed. Please note the following instructions. There will be a ten point deduction for failure to comply with them:

- start each problem on a new sheet of paper
- write your social security number, but not your name, on each sheet of paper you turn in
- show your work whenever appropriate. There can be no partial credit unless I see how answers were arrived
- be succinct. You may lose points for facts that, while true, are not relevant to the question at hand

You have until 12:30 to finish the exam. The questions are equally weighted.

1. Would it be possible to add predicated instructions to an otherwise-conventional RISC-style instruction set? Why or why not?
2. A common feature in early pipelined RISC processors (such as RISC or MIPS) is “forwarding” between instructions. Forwarding avoids pipeline stalls by providing extra data paths between pipeline stages. Forwarding is much less common with more recent superscalar out-of-order processors such as the Pentium 4.

Why is forwarding not as important with these more recent processors?

3. Suppose you have a computer system with a 64 K byte, 2-way set-associative data cache with a 16 byte line using LRU replacement, and you are executing the following code:

```
for (i = 0; i < 1024; i++)  
    a[i] = b[i] + c[i];
```

By an extraordinarily bad coincidence, array *a* starts at address 0x00010000, *b* starts at address 0x00020000, and *c* starts at 0x00030000. *a*, *b*, and *c* are all arrays of 4-byte integers.

- (a) Estimate the hit rate in the data cache.
 - (b) What happens to the hit rate if you add a single, one-line victim cache to the data cache?
4. Suppose we have the following situation on an Alewife machine:
 - Variable *x* is homed on processor P_1 (*ie*, its directory entries are in P_1 's memory controller), is in read-only mode, and has a processor set consisting of $\{P_1, P_3\}$.
 - Variable *y* is homed on processor P_2 , is in read-write mode, and has a processor set consisting of $\{P_1\}$.

Now suppose processor P_2 executes the following line of code:

```
x = y;
```

What messages will be sent among the processors as a result of this statement?

5. For both parts of this problem the CRC polynomial will be $x^2 + 1$.
- (a) Draw a picture of the shift-register implementation of this polynomial.
 - (b) Find the CRC remainder for the message $x^7 + x^5 + x^4 + x^1 + 1$ (you can calculate this any way you want – either doing a division or simulating the shift-register is fine).
6. In a multidimensional toroid, it would be possible to define a “never negative” routing rule: that is, in this scheme, a packet is never routed in a negative direction in any dimension. Would such a routing rule succeed in preventing deadlocks if wormhole routing were being used? Why or why not?