

# A VLSI RISC

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# Motivation

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"Delay-power penalty of data transfers across chip boundaries and the still-limited resources (devices) available on a single chip are major design limitations."

# Constraints

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- ▷ Execute one instruction per machine cycle
- ▷ Make all instructions the same size
- ▷ Access memory only with load and store instructions; the rest operate between registers
- ▷ Support high level languages

# High Level Language Support

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- ▷ Language supported: C
- ▷ Hardware support only for most time-consuming events; rest in software

## Dynamic percentage of operands

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	C1	C2	C3	C4	Avg
Integer Constant	25	11	29	28	20
Scalar	37	45	66	62	55
Array/Structure	36	43	5	10	25

## Relative Frequency of HLL Statements

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Statements	HLL (occur)	Weighted (mach inst)	Weighted (mem r
Call/return	12	33	45
Loops	3	32	26
Assign	38	13	15
If	43	11	13
Case	<1	1	1
Goto	3	0	0

# Instructions

Op code	S	Dest	Src 1	I	Src 2
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**Add**      $Rd \leftarrow Rs + S2$

**Ldl**      $Rd \leftarrow M[Rx + S2]$

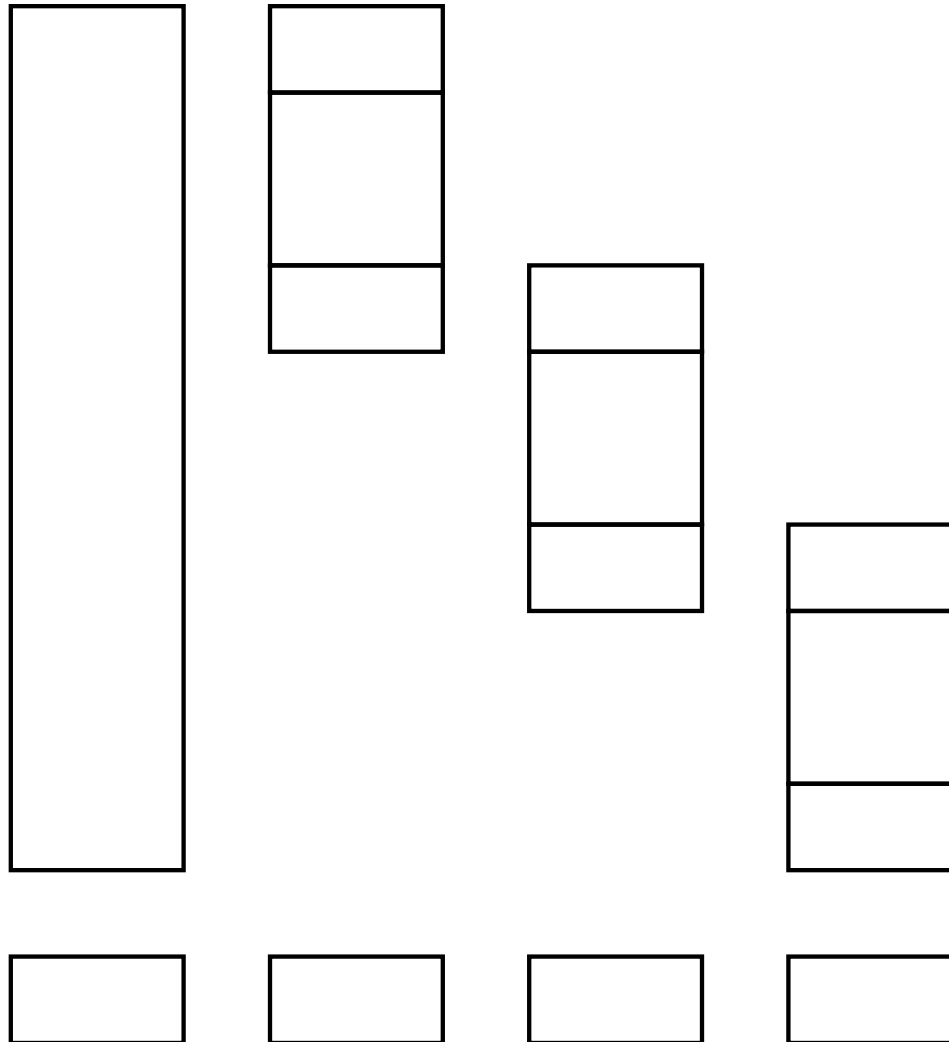
**Jmp**      $PC \leftarrow Rx + S2$

**Call**      $Rd \leftarrow PC, \text{ next } PC \leftarrow Rx +$   
 $CWP \leftarrow CWP - 1$

**Ret**      $PC \leftarrow Rm + S2$   
 $CWP \leftarrow CWP + 1$

# Register Windows

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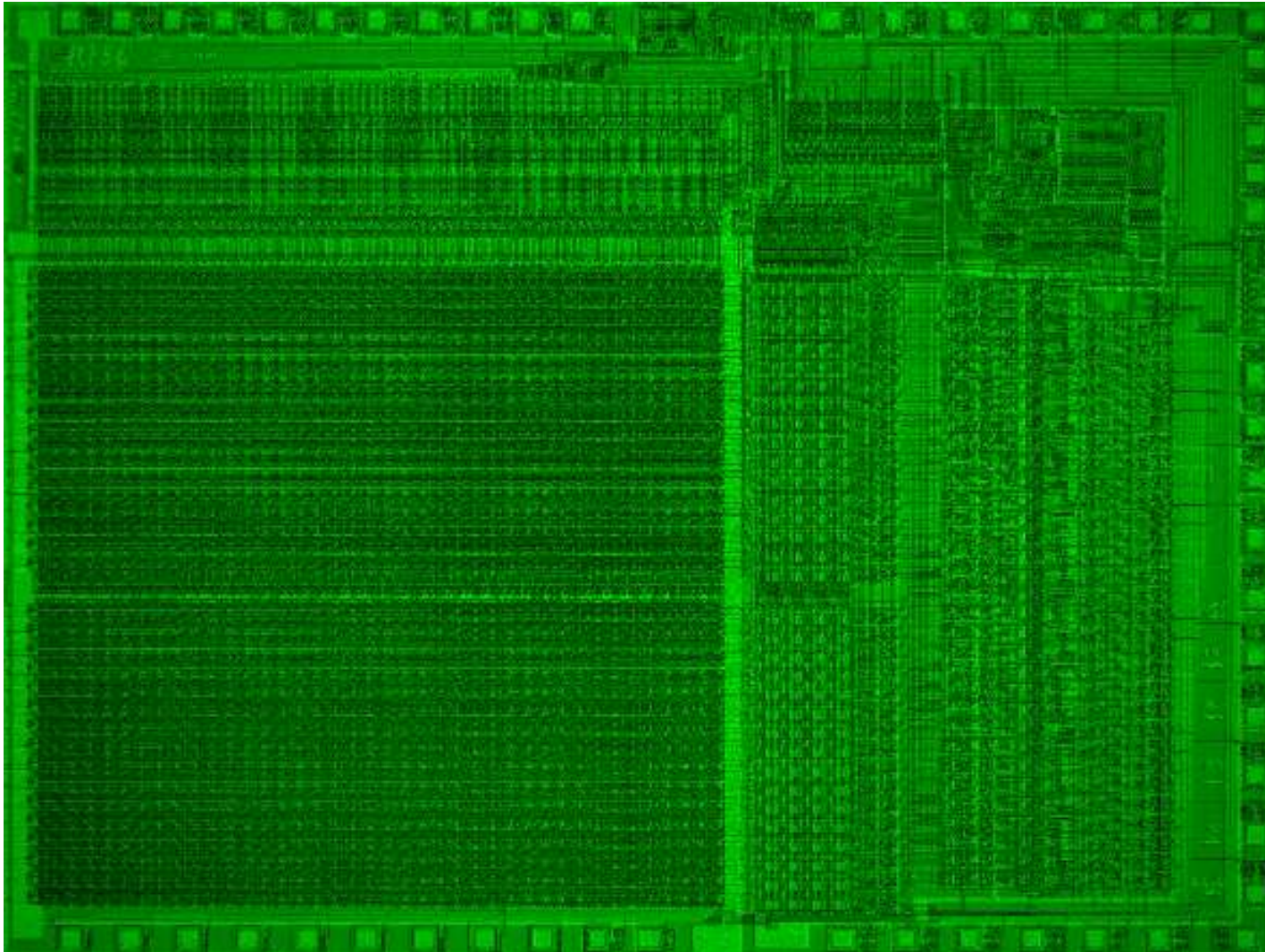
## Call/Return Memory Traffic

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	Calls + Returns	Max Depth	Mem Traffic	
			RISC	VAX
Puzzle	0.7%	20	8K	444K
Quicksort	8.0%	10	4K	696K

# RISC I

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